A 1.2 V 34 µW SECOND ORDER ΣΔ ADC IN 0.13 µM CMOS FOR I-UWB RECEIVER

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ABSTRACT

Analog to Digital converters are key to modern mixed signal circuit designs. Sigma-Delta (□□) modulators form part of the core of today's mixed signal designs. Nyquist Samplers require a complicated analog low pass filter to limit the maximum frequency input to the A/D and Sample and Hold circuit. Sigma-Delta (ΣΔ) modulation based Analog to Digital (A/D) conversion technology is a cost effective alternative for low power, high resolution (greater than 12 bits) converters, which can be ultimately integrated on Digital Signal Processor ICs. In this paper Over Sampling concept is used to address the problem of power dissipation, noise in ADCs and investigating the possibilities of utilizing alternative methods to reduce the noise and power dissipation in ADC architectures. This is achieved by design techniques namely Over Sampling, Second order Sigma-Delta architectures and Switched Capacitor based Sample & Hold circuits.

A Second order Sigma-Delta Modulator is implemented using CMOS 0.13 µm technology using a 1.2 V power supply. Over sampling ratio are 128 with clock frequency of 50 GHz which gives bandwidth of 20 GHz. The total power dissipation of the modulator is 34 µW. The area occupied by the modulator is 25 µm x 30 µm.

KEYWORDS: Analog to Digital Converter (ADC), Sigma-Delta Modulator, Integrator, Over Sampling, Sample and Hold Circuit, Switched Capacitor and Ultra Wide Band (UWB)